Remarks and Arguments

1. Claims 1 – 19 have been rejected under 35 U.S.C. 102(e) as being

5   anticipated by Pekkala (US 2002/0172195) hereinafter Pekkala '195.

Applicant notes that the Office Action infers that the currently pending claims can be distinguished over the art of record by further clarifying the ability of the bus emulator to support a single transaction at a time. Applicant has

10   taught that "In some embodiments of the present invention, the bus emulator may further comprise an arbiter that grants access to the internal bus to one of a plurality of point-to-point interfaces when simultaneous bus requests are pending" (specification Page 5, Lines 8 – 11). Applicant has amended Claims 1, 5, 11, 14 and 17 to further clarify a present feature in accord with the

15   inference made in the Office Action such that the bus emulator can only support one transfer at a time. As such, the Applicant believes that the amended claims address the concerns raised in the currently operative Office Action.

20   Here, Pekkala does teach a point-to-point link as the Office Action notes. However, Pekkala introduces the concept of a transaction switch (302 in Fig. 3). In the claimed invention, each point-to-point link interfaces to a bus emulator. A bus emulator is entirely distinct from Pekkala's transaction switch. Accordingly, Applicant submits that the rejection of Claims 1 – 19

25   under 35 USC 102(b) must be withdrawn.

According to Applicant's teachings, the each local bus is converted to a point-to-point link. Each point-to-point link is communicatively coupled to the bus emulator. The bus emulator, as described by Applicant on Page 9, Lines 9 –

30   12) includes an internal bus with which all point-to-point interfaces are

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communicatively coupled to. As such, this internal bus really is a bus where only one transfer can be accommodated at any given time.

5 In Pekkala, the transaction switch includes, according to Fig. 4, shared memory 404 and multiplexers 402,406. Transfer of data through the transaction switch is accomplished under control of control logic 408 also included in the transaction switch. The transaction switch provides multiple data paths that can be used concurrently to pass transactions from port to port. In other words, the transaction switch is akin to a network switch rather

10 than to a computer bus. The problem with this is that a network switch necessarily introduces latency and a non-deterministic manner of operation when one bus master needs to communicate with a memory mapped device on a different bus. As Applicant claims, the bus emulator is a bus that can have contention as different point-to-point interfaces vie for access to the bus.

15 This results in a more deterministic access profile and prevents out-of-sequence access across the bus.

With respect to Claims 2, 3, and 4 which are dependent on Claim 1; Claims 6, 7, 8, 9, 10 which are dependent on Claim 5; Claims12 and 13 which depend on Claim 11; and Claims 15 and 16 which depend on Claim 14; and Claims

20 18 and 19 which depend on Claim 17, Applicant submits that these claims are dependant on independent claims that Applicant has amended and now believes to be distinguished over the art of record. Accordingly, rejections of these independent claims ought to be withdrawn and Applicant kindly

25 requests such withdrawal.

Specifically, the Office Action purports that Pekkala discloses a bus emulator in Paragraph [0166]. This is not true, in Paragraph [0166] Pekkala discloses the use of a transfer switch, which the entire teaching of Pekkala clearly

30 defines as a true switch, not a bus as Applicant has taught.

The Office Action purports that Pekkala teaches converting received bus signals to a native form in Paragraph [0169]. This again is not true. In Paragraph [0169], Pekkala teaches the transfer of information from a PCI bus into a buffer, not conversion to a native form.

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With respect to Claim 2, The Office Action also purports that Pekkala teaches monitoring native bus cycles (supposedly in Paragraph [0008] and [0166]). This is simply not true. In Paragraph [0008], Pekkala describes at a top level a recent technology called InfiniBus – no where is there a description of

10   monitoring native bus signals to identify a start of a bus cycle.

With respect to Claim 3, the Office Action purports that Pekkala teaches (Paragraphs [0166] and [005]) reception of bus signals from a first point-to-point interface in the bus emulator. This again is simply not true. In

15   Paragraph [0166], Pekkala disclosure teaches the capture of bus signals in a buffer, not propagation of the signals (conveying) onto the bus as claimed by ·Applicant. In fact, in Pekkala, signals from the point-to-point interface are not conveyed to the bus at all, they are used to capture information into a buffer.

20   With respect to Claim 4, the Office Action purports that Pekkala teaches propagating signals onto the bus if the bus structure is granted to the point-to-point interface. In again is not true. In Paragraph [0150], Pekkala does not even talk about granting of a bus structure to a point-to-point link. Applicant rebuts the Office Actions' assertion by noting that Pekkala clearly states in

25   Paragraphs [0072] and [0073] that device communicate through the transaction switch and that the transaction switch includes input and output buffers so that no latency is imparted onto a data transfer. There is simply no mention of arbitration throughout the teachings of Pekkala.

With respect to Claim 7, Pekkala simply does not teach the use of a high-current driver as the Office Action purports. Pekkala's reference in Paragraph [0010] to a multiple IB channel adapter is simply not even remotely equivalent to a high-current adapter. Multiple IB ports are devices that are uniquely

5   identified. How does this constitute a high-current driver?

With respect to Claim 8, Pekkala does not disclose an internal bus. Paragraph [0008] again discloses the prior art of an Infini-Band Architecture and nothing more. There is no mention of an internal bus.

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With respect to Claim 9, Applicant has already demonstrated that Pekkala does not disclose arbitration and granting of access to an internal bus.

With respect to Claim 10, Pekkala does not teach a cascade port to extend an

15   internal bus as the Office Action purports. Pakkala never describes an internal bus that can be extended by means of a cascade port.

With respect to Claim 13, Applicant has already demonstrated that Pekkala does not disclose high-current drivers.

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With respect to Claim 15, the Office Action purports that Pekkala teaches that a serial output is generated once a data field and an address field are accepted from a computer module interface. This is not true. Pekkala, in Paragraph [0166], simply teaches that address and data are accepted into a

25   buffer. There is no mention of generation of a serial output.

With respect to Claim 16, Applicant has already demonstrated that Pekkala does not disclose high-current drivers.

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With respect to Claim 17, Applicant has already demonstrated that Pekkala does not teach the use of an internal bus. The Office Action is simply wrong with respect to what an "IBA" is. IBA is not an internal bus, it is a structure that includes a transfer switch as taught throughout Pekkala.

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With respect to Claim 18, Applicant has already demonstrated that Pekkala does not teach the use of an arbiter. In fact, this would be contrary to Pekkala's teachings wherein input and output buffers are employed to eliminate latency.

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With respect to Claim 19, Applicant has already demonstrated that Pekkala does not teach the use of a bus; ergo, a cascade device can not be applied to extend a bus that does not exist.

15   2. Applicant notes that, to support a rejection of a claim under 35 USC 102, a cited reference must explicitly teach the claimed method and apparatus. Applicant has demonstrated that the only cited reference, Pakkala, fails to teach any requisite features of the claimed invention. Pekkala discloses a system that appears similar only at a very high level, but that is where the

20   equivalence of Pekkala ends. Pekkala teaches a transaction-oriented computer interconnection system. The claims invention is a method and apparatus that enables extension and distal interaction of computer modules on a cycle-by-cycle basis.

25   3. Based on the foregoing, Applicant considers the present invention to be distinguished from the art of record. Accordingly, Applicant respectfully solicits the Examiner's withdrawal of the rejections raised in the above referenced Office Action, such that a Notice of Allowance is forwarded to Applicant, and the present application is therefore allowed to issue as a

30   United States patent.

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Respectfully submitted,

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Jack I. J'maev
Attorney for Applicant
Reg. No. 45,669

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Intellectual Property Development
PO Box 3156
Fullerton, CA 92834
15   Phone 909-437-8390

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